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OSCILLATOR CIRCUIT WITH VARIABLE REFERENCE VOLTAGE AND CURRENT

Field of the Invention

The invention is related to oscillators, and in particular, to a relaxation oscillator circuit that employs a variable reference voltage and current.

Background of the Invention

Oscillator circuits are used in computers, computer peripherals, counters, timers, calculators, phase-locked loops, digital multimeters, oscilloscopes, and numerous other applications. An oscillator circuit may be used to provide a clock signal, to produce an accurate waveform, and the like.

A type of oscillator circuit referred to as a relaxation oscillator generally operates as follows. The relaxation oscillator charges a capacitor with a reference current, and discharges the capacitor rapidly if the capacitor voltage reaches a reference voltage. The charging and discharging of the capacitor generates a sawtooth waveform that is used to generate the output signal. Alternatively, the polarity of the current may be reversed when the reference voltage is reached, generating a triangle waveform rather than a sawtooth waveform.

Also, the reference voltage is typically provided by a bandgap reference, so that the reference voltage is substantially independent of temperature and supply voltage. The current used to charge the capacitor is also typically substantially independent of temperature and supply voltage. In this way, the oscillator frequency can be substantially independent of variations in temperature and supply voltage.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

FIGURE 1 shows a block diagram of an embodiment of an oscillator circuit;

FIGURE 2 schematically illustrates an oscillator circuit that is an embodiment of the oscillator circuit of FIGURE 1;

FIGURE 3 shows a waveform of an embodiment of the reference current of FIGURE 2; and

FIGURE 4 illustrates a timing diagram of waveforms of embodiments of signals from the oscillator circuit of FIGURE 2, in accordance with aspects of the invention.

Detailed Description

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, and the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The phrase "in one embodiment," as used herein does not necessarily refer to the same embodiment, although it may. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, a relaxation oscillator circuit is configured to provide an output signal. The relaxation oscillator circuit includes two capacitors that are alternatively charged and discharged. Each capacitor is charged by a separate current that is provided

by mirroring a reference current. The reference current for the current mirror may be provided by a bias circuit such that the reference current may vary significantly over temperature and supply voltage. Also, substantially the same reference current is mirrored to a resistor to provide the reference voltage. The resistor has a temperature coefficient that is substantially zero. Accordingly, the output signal is relatively independent of temperature and supply voltage, even though the reference current and the reference voltage may vary substantially over temperature and supply voltage.

FIGURE 1 shows a block diagram of an embodiment of oscillator circuit 100. Oscillator circuit 100 includes components such as current mirror circuit 110, current source circuit 120, switch circuits 131-132, capacitors C1-C2, constant resistance circuit 140, and switch control circuit 150.

In operation, current source circuit 120 provides reference current I1. Current mirror circuit 110 is configured to provide currents I2, I3, and I4 from reference current I1. Also, the currents I2 and I3 are configured to be substantially equal to each other.

Also, switch circuit 131 and capacitor C1 are arranged such that capacitor C1 is charged by current I2 if an output signal (OUT) corresponds to a first logic level, and discharged if signal OUT corresponds to a second logic level. Conversely, switch circuit 132 and capacitor C2 are arranged such that capacitor C2 is charged by current I3 if signal OUT corresponds to a second logic level, and discharged if signal OUT corresponds to a first logic level. Further, capacitor C1 is arranged to provide signal VC1, and capacitor C2 is arranged to provide signal VC2.

Additionally, constant resistance circuit 140 is configured to provide reference voltage VREF from current I4. More specifically, constant resistance circuit 140 is configured to provide VREF such that VREF=I4*R0, and such that R0 is substantially independent of temperature and supply voltage.

Because R0 is substantially independent of temperature and supply voltage, reference voltage VREF tracks any variations in current I4 that result from changes in temperature and supply voltage.

In one embodiment, current source circuit 120 is a variable current source circuit. In this embodiment, current I1 can vary significantly over temperature and supply voltage.

Also, switch control circuit 150 is configured to provide output signal OUT and an inverse of signal OUT (OUTB) from signals VC1, VC2, and VREF. Further, circuit 100 is arranged such that signal OUT is substantially independent of supply voltage and temperature, regardless of whether reference current I1 varies with supply voltage and/or temperature.

FIGURE 2 schematically illustrates an embodiment of oscillator circuit 200. Components in oscillator circuit 200 may operate in a similar manner to similarly-named components in oscillator circuit 100, and may operate in a different manner in some ways. Oscillator circuit 200 includes current mirror circuit 210, variable current source circuit 220, switch circuits 231-232, capacitors C1-C2, constant resistance circuit 240, and switch control circuit 250. Oscillator circuit 200 may also include capacitor C3. An embodiment of current mirror circuit 210 includes transistors M1-M4. Also, an embodiment of current source circuit 220 includes transistor M5-M7 and resistors R1-R2. An embodiment of switch circuit 231 includes switches S1-S2. Similarly, an embodiment of switch circuit 232 includes switches S0 and S3. An embodiment of constant resistance circuit 240 includes resistor R0. In addition, an embodiment of switch control circuit 250 includes comparators CMP1-CMP2 and SR latch 254.

In operation, variable current source circuit 220 provides reference current I1. More specifically, variable current source circuit 220 is configured to provide reference current I1 such that reference current I1 varies significantly over temperature and supply voltage (VDD). Also, resistors R1 and R2 may be pre-selected to provide the desired amount of current for reference current I1.

FIGURE 3 shows an embodiment of a waveform (370) of an embodiment of current I1. As shown, current I1 varies significantly with supply voltage (VDD). In one embodiment, current I1 varies from approximately 1.7 μA to 2.3 μA over a range of approximately 2.2V to 6.0V for VDD.

Referring back to FIGURE 2, current mirror 210 is configured to provide currents I2-I4 from current I1. Accordingly, currents I2-I4 also vary significantly with temperature and supply voltage (VDD).

Also, capacitor C1 and switches S1 and S2 are arranged to provide voltage VC1 as follows. If signal OUT is low, switch S1 is closed and switch S2 is open, which

causes capacitor C1 to charge. This in turn causes voltage VC1 to increase linearly at a rate of approximately I2/C1. Conversely, if signal OUT is high, switch S1 is open and switch S2 is closed, which causes capacitor C1 to discharge. This in turn causes voltage VC1 to return to approximately zero volts.

Similarly, Capacitor C2 and switches S0 and S3 are arranged to provide voltage VC2 as follows. If signal OUT is high, switch S0 is closed and switch S3 is open, which causes capacitor C2 to charge. This in turn causes voltage VC2 to increase linearly at a rate of approximately I3/C2. Conversely, if signal OUT is low, switch S0 is open and switch S3 is closed, which causes capacitor C2 to discharge. This in turn causes signal VC2 to return to return to approximately zero volts.

Additionally, resistor R0 is configured to provide signal VREF from current I4 such that VREF=I4*R0. Further, resistor R0 is configured to have a resistance that is substantially constant regardless of temperature and supply voltage.

Resistor R0 has a temperature coefficient of substantially zero. In one embodiment, resistor R0 is a series combination of two or more different types of resistors having different temperature coefficients. In one embodiment, resistor R0 includes a series combination of two resistors, the first having a positive temperature coefficient, and the second having a negative temperature coefficient. In one embodiment, resistor R0 includes poly-silicon having a positive temperature coefficient, and high-resistance poly-silicon having a negative temperature coefficient. Preferably, the resistance of resistor R0 is selected such that VREF remains substantially within the supply voltage rails.

Also, one embodiment of switch control circuit 250 is arranged to operate as follows. Comparator CMP1 is configured to compare voltages VC1 and VREF, and to provide signal VINS in response to the comparison. Similarly, comparator CMP2 is configured to compare voltages VC2 and VREF, and to provide signal VINR in response to the comparison. SR latch 254 is configured to provide signals OUT and OUTB from signals VINS and VINR. Although one embodiment of switch control circuit 250 is discussed, other embodiments are within the scope of the invention. In one embodiment, SR latch 254 may be replaced with another circuit, such as a different type of latch, a

flip-flop, and the like. In one embodiment, the two comparators and the latch may be with a double-differential latching comparator or with two latching comparators.

Additionally, capacitor C3 is an optional component of oscillator circuit 200. Capacitor C3 may prevent fast transients in voltage VREF.

FIGURE 4 illustrates a timing diagram of waveforms of embodiment of signals VC1, VC2, and OUT for oscillator circuit 200. As shown in FIGURE 4, if signal OUT is high, voltage VC2 ramps upwards until voltage VC2 reaches voltage VREF. When this happens, comparator CMP2 asserts signals VINR, which resets SR latch 254. This in turn change signal OUT to change to low. When this happens, voltage VC2 is reduced to substantially zero, and voltage VC1 beings ramping upwards. Voltage VC1 ramps upwards until voltage VC1 reaches voltage VREF. When this happens, comparator CMP1 asserts signal VINS, which sets SR latch 254. This in turns changes signal OUT to high. When this happens, voltage VC2 begins ramping upwards again.

In one embodiment, C1 is substantially equal to C2. In this embodiment, the frequency of oscillation f associated with signal OUT is substantially given by f=I1/(2*C*VREF), where C=C1=C2. Accordingly, f=1/(2*R0*C*k), where k is the mirror ratio between transistors M3 and M4.

Accordingly, the frequency of oscillation associated with signal OUT depends on R0 and C. The frequency of oscillation is substantially independent of supply voltage and temperature.

Preferably, comparators CMP1 and CMP2 are each configured to perform their respective comparisons within a time interval of 1% of the desired period of oscillation or less.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.